AMENDMENTS TO THE SPECIFICATION

Please amend the specification as shown below.

Please amend the paragraph beginning on page 3, line 24, and continuing on page 4 with the following new paragraph:

To attain the above object, according to the present invention, there is provided a clock switching circuit for receiving as an input a plurality of clock signals including [a] first and second clock signals and switching one clock signal to be output from the first clock signal to the second clock signal, comprising a plurality of unit circuits for respectively receiving as an input the clock signals, selection signals of the clock signals and enabling signals and controlling supplying and stopping of the clock signals in accordance with the selection signals and the enabling signals; and a feedback circuit for monitoring output conditions of the plurality of unit circuits and, when outputting of all clock signals of the plurality of unit circuits was stopped as a result of stopping the first clock signal, giving a plurality of the unit circuits the enabling signals for approving starting of a supply of the second clock signal.

Please replace the paragraph beginning on page 4, line 17, and continuing on page 5 with the following new paragraph:

Assuming that in accordance with a selection signal input to a unit circuit corresponding to a first clock signal, the first clock signal is output from the unit circuit. At this time, [other] another unit circuit corresponding to a second clock signal does not output a clock signal. Next,

logic states (voltage levels) of two selection signals of the two are inversed and an instruction that a clock signal to be output is switched from the first clock signal to the second clock signal is given. The unit circuit outputting the first clock signal stops outputting the first clock signal. A feedback circuit detects that the first clock signal is stopped and gives an enabling signal to the above plurality of unit circuits. A unit circuit corresponding to the second clock signal starts to supply the second clock signal due to an input of the enabling signal.

Please replace the paragraph beginning on page 10, line 22, and continuing on page 11, with the following new paragraph:

In the delay unit 10b, the monitor signal "cken_x" for a clock output condition is generated by the OR gate 15 by obtaining a logical sum of the output of the flip-flop 11 and the output of the flip-flop 12. When the selection signal "sel_x" input to the unit circuit 10-x shifts from a level indicating a selected state to a level indicating a non-selected state, after the output of the flip-flop 11 as the enabling signal "enout" of the clock gating becomes "L", the monitor signal "cken_x" is shifted to "L" by being delayed exactly by one clock cycle. Due to this, continuation of a clock signal for at least [last] one cycle is guaranteed from a reception of an instruction to stop the clock signal until an actual stopping of the clock signal.

AMENDMENTS TO THE DRAWINGS

One (1) attached sheet of drawing includes changes to Fig. 3, Fig. 3H and Fig. 3I. The changes to these Figures are as follows.

Sheet 1 includes Fig. 3, Fig. 3H and Fig. 3I. Fig. 3 has been modified to change the time signal "T6" to -- T5 --; Fig. 3H has been modified to change "ckout_m" to -- CLKOUT_M -- and Fig. 3I has been modified to change "ckout_n" to -- CLKOUT_N --.

Attachment: One (1) Replacement sheet